**All Digital Phase Locked Loop (ADPLL) Design for Transceiver System**

**Introduction**

This project is about digital phase locked loop desinging on QAM Transceiver System. In this project we analyze and work on different types of DPLL systems. After the anaylzation system we will list the advantages and disadvantages of different DPLL systems and compare these systems. These comparations is all about performance ratings and error rates. Finally with these observations we hope to achieve the optimum FPGA tranciever system and its place in communication systems.

1. **ADPLL Design**

Recently digital PLLs are attracting more attention for the significant advantages of digital systems over their analog counterparts. These advantages include superiority in performance, speed, reliability, and reduction in size and cost. Analog PLLs biggest disadvantage is voltage controlled oscillator and a loop filter since it creates sensitivity of temprature and power supply variations. DPLLs do not suffer from such a problem. Also DPLLs has larger time for better frequency resolution, and this will reduce the locking speed. In order to do that DPLLs use Phase Detectors (PD) to lock the filter loops and continue the specified application.

The DPLLs can be classified according to the mechanizationof the phase detector into four types as follows

**1.1)Flip Flop PD**

The PD counts the number of high-frequency clock periods between the phase difference of v1 and v2 as shown in Figure.1.

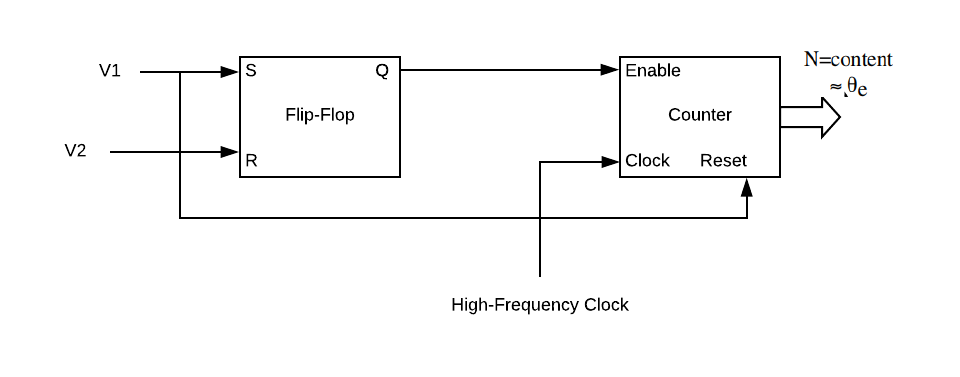


Figure.1

**1.2)Hilbert Transform Phase Detector**

The Hilbert Transform based Phase Detector (HTPD), which employs quadrature signal processing method, estimates phase difference between input and output signals without using LP filter. It offers an excellent noise immunity compared to other techniques. Its block diagram can be shown in Figure.2.

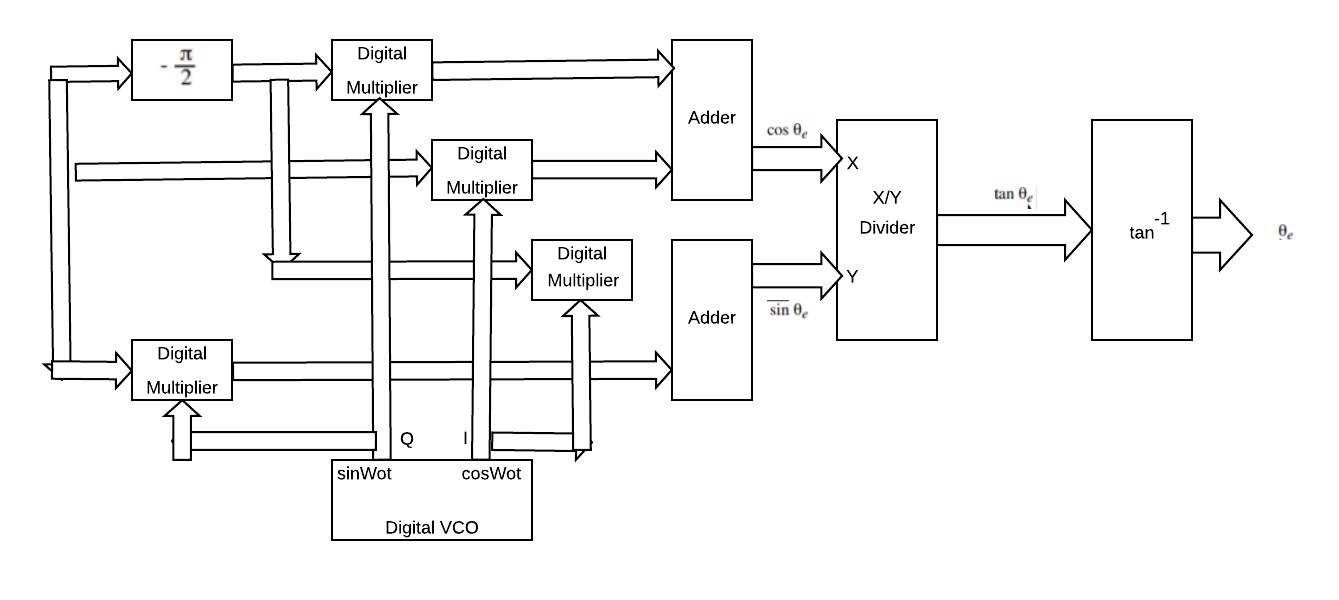


Figure.2

**1.3)Digital-Averaging Phase Detector**

Similar to the Hilbert transform but simpler. Cosine and Sine outputs of adders are implemented by averaging(integrating) the output signals of the multipliers over an appropriate period of time. This phase detector includes a filter function defined by the impulse function of the averaging circuitry that can be observed in Figure.3.

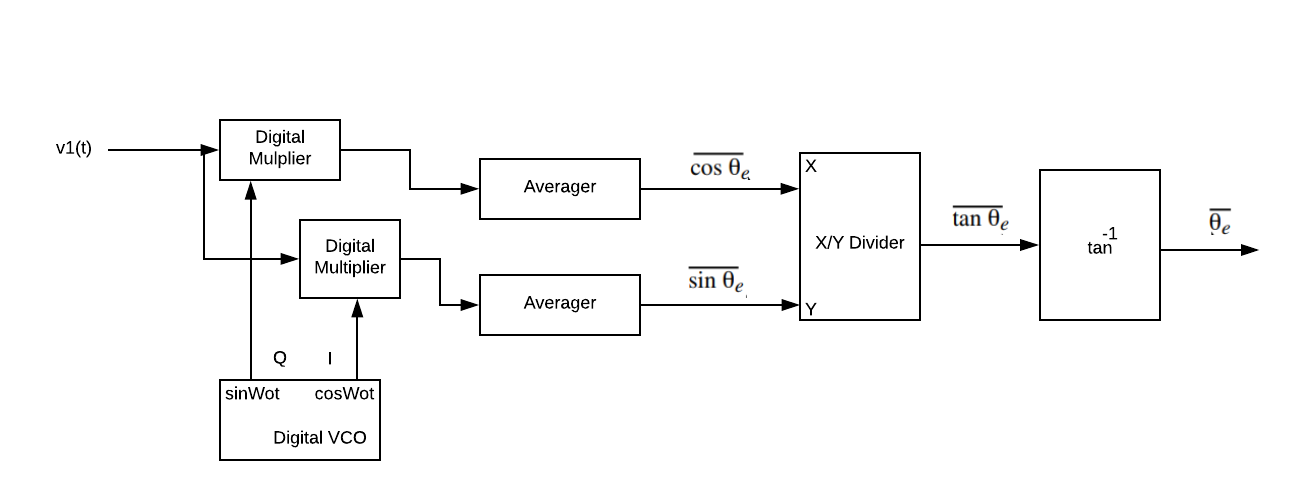


Figure.3

**1.4)EXOR Phase Detector**

It comprises of a logic exclusive OR circuit. Being digital in format it can often fit into a phase locked loop with ease as many of the circuits associated with the phase locked loop may already be in a digital format. In Figure.4 PD can be observed including with JK-Flip-Flop detector.

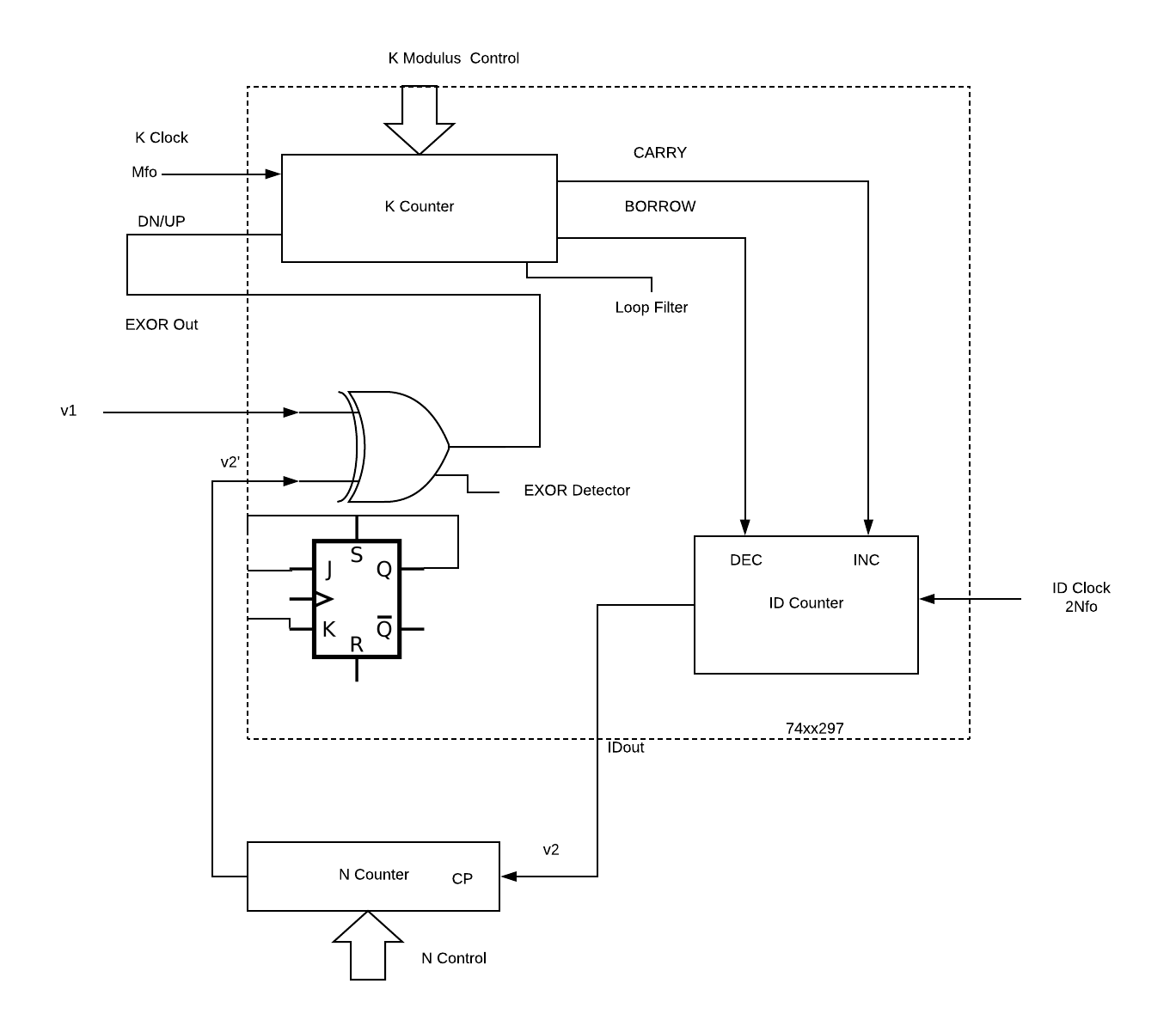


Figure.4

1. **QAM Transciever**

In digital communications QAM is widely used technique since it has high bandwidth efficiency than other modulation types. In Figure.5 QAM modulator block diagram can be observed. With using Square Root Raise Cosine Filter, QAM inputs can be generating and reduces the Inter Symbol Interference(ISI). After the multiplication operation with carrier QAM transmitter signal can be send through the communication channel as the sum of the in phase and quadratic phase outputs.

QAM demodulator block diagram can be observed in Figure.6. Inverse process of modulation has to be done on the demodulator. In order to do that demodulator has to use original information content from the modulated carrier wave. In demodulator matched filter is used. However it can’t combine the input samples with decimation factors since PLL needs it for synchronization. In this project QAM receiver uses the DPLL circuitary in order to synchronize the receiving signal and analyze the order of it.

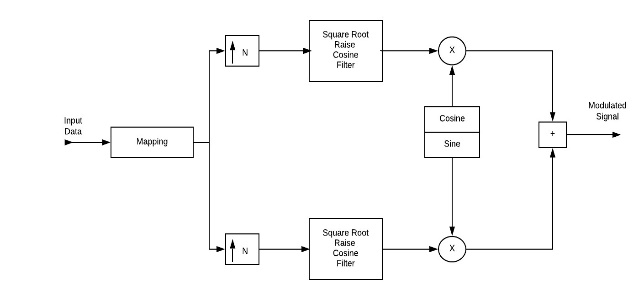
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Figure.5

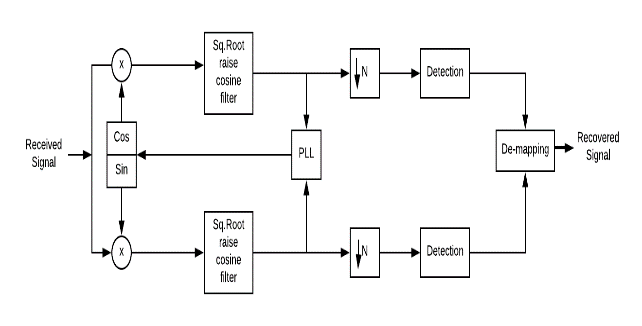


Figure.6

1) Implementing square root cosine filter on Matlab.

2) Building QAM Transmitter system on the Matlab and observing varying data vectors information on transmitter output signal.

3) Implemenating square root cosine filter and transmitter system on ISE.

4) Observing the output of transmitter system on oscilloscope.

5) Implementing different PLL systems on Matlab and compare performance and error ratings.

6) Building QAM Receiver system on the Matlab and observing the incoming signals that have been converted through the digital to analog converter.

7) Implementing receiver system with optimum DPLL theory on ISE.

8) Testing the final system with real-time sound and video applicatons.